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(FILE 'USPAT' ENTERED AT 10:45:23 ON 21 OCT 91)
L1 7 S (BACK-UP OR BACKUP)(10W)(PROM)
L2 19 S (BACK-UP OR BACKUP)(20W)(EPROM)
L3 1 S (BACK-UP OR BACKUP)(20W)(NON-VOLITAL)
L4 79 S (BACK-UP OR BACKUP)(20W)(NON-VOLATILE)
L5 2 S L4 AND CACHE
L6 148 S (BACK-UP OR BACKUP)(20W)(VOLATILE)
L7 3 S L6 AND CACHE

=> d l1 1-7 cit,ab

1. 4,965,828, Oct. 23, 1990, Non-volatile semiconductor memory with SCRAM hold cycle prior to SCRAM-to-E.sup.2 PROM backup transfer; Harold L. Ergott, Jr., et al., 380/50; 307/64; 365/229; 371/14; 380/3, 4, 49 [IMAGE AVAILABLE]

US PAT NO: 4,965,828 [IMAGE AVAILABLE] L1: 1 of 7

ABSTRACT:
A non-volatile memory system includes an SRAM and a backup store of E.sup.2 PROMs. In the event of a short duration power interruption, the memory system enters a hold mode in which data maintenance power is supplied to the SRAM by discharging a backup capacitor, and accessing of the SRAM by a host computer is halted. If the backup capacitor voltage does not fall below a threshold before power is restored, the hold mode is terminated and accessing by the host computer continues. If the backup capacitor voltage falls below the threshold, operating power is supplied to the SRAM, E.sup.2 PROM, and associated circuitry to download all data and row and column parity data into the E.sup.2 PROM by further discharging of the backup capacitor. Row parity and column parity information are accumulated by a bit-per-chip accumulation technique that allows convenient error correction on a "per chip" basis. Data is encrypted and decrypted on the basis of a fully erasable magnetic key.

2. 4,931,789, Jun. 5, 1990, Apparatus and method for a universal electronic locking system; Douglas A. Pinnow, 340/825.56, 825.31, 825.69, 825.72 [IMAGE AVAILABLE]

US PAT NO: 4,931,789 [IMAGE AVAILABLE] L1: 2 of 7

ABSTRACT:
An apparatus and method for providing a universal electronic locking system (UELS) which controls an actuating device for a lock is disclosed. The system is composed of two elements, a signal-transmitting unit and a signal-receiving unit. The signal transmitting unit transmits one or more encoded signals on electromagnetic carriers. An integrated circuit includes a programmable memory unit such that various codes may be entered and the codes may be changed at any interval desired by the operator. The signal-receiving unit comprises a means for receiving the encoded signals from the signal-transmitting unit and contains a programmable memory unit which is responsive to each and all codes contained in the signal-transmitting unit. Upon changing the code signal in the signal-transmitting unit, the memory unit of the signal-receiving unit may be reprogrammed so as to be responsive to the newly encoded signal and allow the latching mechanism of the lock system to be operated. The system may be used alone or in combination with conventional key operated locking mechanisms. The UELS is contemplated for applications in the home, business industry, recreation, defense and wherever locks and codes are used.

The system is composed of two elements, a signal-transmitting unit and a signal-receiving unit. The integrated circuit chip of the watch is expanded to include a programmable memory unit such that various codes may be entered in the watch and the codes may be changed at any interval desired by the operator. The signal-receiving unit comprises a photodetector for receiving an optical signal from the signal-transmitting unit and contains a programmable memory unit which is responsive to each and all codes contained in the signal-transmitting unit. Upon changing the code signal in the signal-transmitting unit, the memory unit of the signal-receiving unit may be reprogrammed so as to be responsive to the newly encoded signal and allow the latching mechanism of the lock system to be operated. The system may be used alone or in combination with conventional key operated locking mechanisms. The UELS is contemplated for applications in the home, business, industry, recreation, defense and wherever locks and codes are used.

7. 4,443,865, Apr. 17, 1984, Processor module for a programmable controller; Ronald E. Schultz, et al., 364/900, 916, 916.2, 921, 921.3, 921.8, 921.9, 926, 926.9, 929.2, 929.4, 929.5, 933, 933.6, 933.7, 939, 939.3, 946, 946.2, 946.5, 946.6, 946.9, 948.4, 948.6, 949, 949.1, 954, 954.2, 959, 964, 965, 965.5, 965.76, 965.78, 966.1, 966.5 [IMAGE AVAILABLE]

US PAT NO: 4,443,865 [IMAGE AVAILABLE] L1: 7 of 7

ABSTRACT:
A processor module is one of several modules mounted in a rack to form a programmable controller. The module has a microprocessor that executes a sequence of machine language instructions to interpret and thereby execute macroinstructions that are part of a control program stored in a read/write volatile main memory. The rate of execution is improved by reducing the instructions in a fetch sequence used in coupling each macroinstruction to its interpreter sequence of machine-language instructions. Hardware assistance is provided to allow expansion of macroinstruction operation codes as they are fetched. The processor module also allows the user to program his own interpreter sequences for specially defined macroinstructions and to load these sequences into a nonvolatile memory that is plugged into the module. An external auxiliary power supply is connected to the processor module to supply the programming voltage required by the nonvolatile memory.

=> d l7 1-3 cit,ab

1. 5,031,144, Jul. 9, 1991, Ferroelectric memory with non-destructive readout including grid electrode between top and bottom electrodes; George Persky, 365/145; 357/23.6; 361/301, 321; 365/149 [IMAGE AVAILABLE]

US PAT NO: 5,031,144 [IMAGE AVAILABLE] L7: 1 of 3

ABSTRACT: w3
the bottom electrode. A dielectric material (20) is located immediately between the spaced coducting members of the grid electrode (18) and the top electrode (20). This forms ferroelectric fingers (22) which can be selectively polarized by applying a voltage between the top electrode and the grid electrode during reading of the memory cell (10). When the read operation is complete, the ferroelectric fingers (22) will spontaneously repolarize to the state of the rest of the continuous ferroelectric bulk (16). This results in a ferroelectric memory with nondestructive readout.

2. 4,484,303, Nov. 20, 1984, Programmable controller; Salvatore R. Provanzano, et al., 364/900, 147, 926.9, 927.2, 927.83, 928, 929.2, 933, 933.4, 933.7, 940, 940.1, 940.2, 940.4, 940.61, 940.64, 940.71, 942.3, 942.5, 946.2, 948.3, 948.34, 949, 949.3, 953, 953.4, 962, 964, 964.2, 964.29, 965, 965.4, 965.5, 965.78, 970, 970.5 [IMAGE AVAILABLE]

DATE FILED: Oct. 12, 1988

10. 4,989,206, Jan. 29, 1991, Disk drive memory; Robert H. Dunphy, Jr., et al., 371/10.1, 11.1, 40.4 [IMAGE AVAILABLE]

US PAT NO: 4,989,206 [IMAGE AVAILABLE] L2: 10 of 30
DATE FILED: Jan. 11, 1990

11. 4,989,205, Jan. 29, 1991, Disk drive memory; Robert H. Dunphy, Jr., et al., 371/10.1; 364/200; 371/40.1 [IMAGE AVAILABLE]

US PAT NO: 4,989,205 [IMAGE AVAILABLE] L2: 11 of 30
DATE FILED: Jan. 11, 1990

12. 4,987,600, Jan. 22, 1991, Digital sampling instrument; David P. Rossum, 381/118; 84/603, 621 [IMAGE AVAILABLE]

US PAT NO: 4,987,600 [IMAGE AVAILABLE] L2: 12 of 30
DATE FILED: Aug. 3, 1989

13. 4,977,495, Dec. 11, 1990, System and method for accessing a cache memory which is located in the main memory of a large data processing system; William Stratton, et al., 364/200, 243.41, 248.1 [IMAGE AVAILABLE]

US PAT NO: 4,977,495 [IMAGE AVAILABLE] L2: 13 of 30
DATE FILED: Feb. 29, 1988

14. 4,965,717, Oct. 23, 1990, Multiple processor system having shared memory with private-write capability; Richard W. Cutts, Jr., et al., 364/200, 228.1, 228.3 [IMAGE AVAILABLE]

US PAT NO: 4,965,717 [IMAGE AVAILABLE] L2: 14 of 30
DATE FILED: Dec. 13, 1988

15. 4,959,860, Sep. 25, 1990, Power-on password functions for computer system; Jeffrey S. Watters, et al., 380/4, 25 [IMAGE AVAILABLE]

US PAT NO: 4,959,860 [IMAGE AVAILABLE] L2: 15 of 30
DATE FILED: Feb. 7, 1989

16. 4,943,983, Jul. 24, 1990, Subscriber unit for wireless digital telephone system; David N. Critchlow, 375/84, 8, 56, 67 [IMAGE AVAILABLE]

US PAT NO: 4,943,983 [IMAGE AVAILABLE] L2: 16 of 30
DATE FILED: Oct. 12, 1988

17. 4,914,656, Apr. 3, 1990, Disk drive memory; Robert H. Dunphy, Jr., et al., 371/10.2, 40.1, 40.4

US PAT NO: 4,914,656 L2: 17 of 30
DATE FILED: Jun. 28, 1988

18. 4,910,706, Mar. 20, 1990, Analog memory for storing digital information; Gilbert P. Hyatt, 365/45, 189.01, 222, 230.01 [IMAGE AVAILABLE]

US PAT NO: 4,910,706 [IMAGE AVAILABLE] L2: 18 of 30
DATE FILED: Aug. 4, 1983

19. 4,905,196, Feb. 27, 1990, Method and storage device for saving the computer status during interrupt; Hubert Kirrmann, 365/200, 75 [IMAGE AVAILABLE]

US PAT NO: 4,905,196 [IMAGE AVAILABLE] L2: 19 of 30
DATE FILED: Oct. 5, 1987

29. 4,445,189, Apr. 24, 1984, Analog memory for storing digital information; Gilbert P. Hyatt, 364/600, 862; 365/45, 183; 446/302, 484

US PAT NO: 4,445,189 L2: 29 of 30
DATE FILED: Jun. 19, 1980

30. 4,307,447, Dec. 22, 1981, Programmable controller; Salvatore R. Provanzano, et al., 364/200, 221.9, 222, 228.5, 230, 230.3, 231.4, 231.6, 231.8, 232.7, 234, 234.4, 238.3, 242, 242.1, 242.3, 242.94, 243, 243.4, 243.41, 244, 244.3, 244.8, 244.9, 245, 245.1, 254, 254.3, 255.1, 255.2, 255.3, 260.4, 260.7, 261, 262, 262.1, 265, 267, 267.4, 270, 270.3, 280, 280.8 [IMAGE AVAILABLE]

US PAT NO: 4,307,447 [IMAGE AVAILABLE] L2: 30 of 30
DATE FILED: Jun. 19, 1979

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1. 5,053,761, Oct. 1, 1991, Method for smooth bitmap scrolling; John W. Webster, III., 340/726, 724, 799 [IMAGE AVAILABLE]

US PAT NO: 5,053,761 [IMAGE AVAILABLE] L2: 1 of 30
DATE FILED: Jun. 16, 1989

2. 5,020,999, Jun. 4, 1991, Personal computer with connector assembly having integral retainer; John R. Dewitt, et al., 439/328; 364/200; 439/377 [IMAGE AVAILABLE]

US PAT NO: 5,020,999 [IMAGE AVAILABLE] L2: 2 of 30
DATE FILED: Jul. 19, 1990

3. 5,014,235, May 7, 1991, Convolution memory; Steven G. Morton, 364/900, 754, 923.5, 927.8, 939.3 [IMAGE AVAILABLE]

US PAT NO: 5,014,235 [IMAGE AVAILABLE] L2: 3 of 30
DATE FILED: Dec. 15, 1987

4. 5,014,125, May 7, 1991, Television system for the interactive distribution of selectable video presentations; Terrence H. Pocock, et al., 358/86, 143; 379/105; 455/4 [IMAGE AVAILABLE]

US PAT NO: 5,014,125 [IMAGE AVAILABLE] L2: 4 of 30
DATE FILED: May 5, 1989

5. 5,010,522, Apr. 23, 1991, Integrated-circuit configuration having fast local access time; Benjamin H. Ashmore, Jr., 365/189.07, 189.05 [IMAGE AVAILABLE]

US PAT NO: 5,010,522 [IMAGE AVAILABLE] L2: 5 of 30
DATE FILED: Nov. 29, 1989

6. 5,008,829, Apr. 16, 1991, Personal computer power supply; Roger L. Cox, et al., 364/480; 363/84, 125 [IMAGE AVAILABLE]

US PAT NO: 5,008,829 [IMAGE AVAILABLE] L2: 6 of 30
DATE FILED: Jun. 14, 1990

7. 5,007,027, Apr. 9, 1991, Data protection system in a data processing system; Hiroyuki Shimoi, 365/229 [IMAGE AVAILABLE]

US PAT NO: 5,007,027 [IMAGE AVAILABLE] L2: 7 of 30
DATE FILED: May 9, 1989

8. 4,996,697, Feb. 26, 1991, Deglitching means for digital communication systems; David N. Critchlow, et al., 375/104; 455/223 [IMAGE AVAILABLE]

US PAT NO: 4,996,697 [IMAGE AVAILABLE] L2: 8 of 30
DATE FILED: Oct. 12, 1988

9. 4,994,802, Feb. 19, 1991, Subscriber unit for wireless digital telephone system; David N. Critchlow, et al., 341/122, 155 [IMAGE AVAILABLE]

US PAT NO: 4,994,802 [IMAGE AVAILABLE] L2: 9 of 30

20. 4,893,317, Jan. 9, 1990, Digital signals and frequency correction in a digital wireless system; David N. Critchlow, et al., 375/97; 328/155; 375/120

US PAT NO: 4,893,317 L2: 20 of 30
DATE FILED: Oct. 12, 1988

21. 4,881,240, Nov. 14, 1989, AM equalizer circuit for digital systems; David N. Critchlow, et al., 375/15; 333/18; 375/13

US PAT NO: 4,881,240 L2: 21 of 30
DATE FILED: Oct. 12, 1988

22. 4,841,474, Jun. 20, 1989, Computer system with work stations at remote positions and reserve battery power supply; Frederik Zandveld, et al., 364/900; 307/66; 364/145, 918, 918.2, 928, 928.3, 943.9, 943.91, 948.4, 948.5, 948.9, 965.78, 965.79; 371/66 [IMAGE AVAILABLE]

US PAT NO: 4,841,474 [IMAGE AVAILABLE] L2: 22 of 30
DATE FILED: May 10, 1985

23. 4,825,448, Apr. 25, 1989, Subscriber unit for wireless digital telephone system; David N. Critchlow, et al., 375/8; 332/103; 375/56, 67

US PAT NO: 4,825,448 L2: 23 of 30
DATE FILED: Aug. 7, 1986

24. 4,819,159, Apr. 4, 1989, Distributed multiprocess transaction processing system and method; Dale L. Shipley, et al., 364/200, 230.6, 236.3, 238.4, 238.5, 239, 239.7, 242.4, 242.6, 242.92, 242.94, 242.95, 244, 244.8, 248.1, 265, 266.3, 267, 267.2, 267.4, 268, 268.3, 268.4, 268.5, 268.7, 268.9, 269.2, 269.3, 280, 281.3, 281.8, 282.1, 282.4; 371/9.1 [IMAGE AVAILABLE]

US PAT NO: 4,819,159 [IMAGE AVAILABLE] L2: 24 of 30
DATE FILED: Aug. 29, 1986

25. 4,811,190, Mar. 7, 1989, Capacitive boost circuit for extending hold up time; Alexander S. Keir, et al., 363/60; 307/110; 363/50 [IMAGE AVAILABLE]

US PAT NO: 4,811,190 [IMAGE AVAILABLE] L2: 25 of 30
DATE FILED: Mar. 3, 1988

26. 4,720,812, Jan. 19, 1988, High speed program store with bootstrap; Ming-Luh Kao, et al., 364/900, 925.6, 964.2, 965.76, 975.2 [IMAGE AVAILABLE]

US PAT NO: 4,720,812 [IMAGE AVAILABLE] L2: 26 of 30
DATE FILED: May 30, 1984

27. 4,493,081, Jan. 8, 1985, Dynamic memory with error correction on refresh; Frederick W. Schmidt, 371/37.3, 13

US PAT NO: 4,493,081 L2: 27 of 30
DATE FILED: Jan. 11, 1984

28. 4,484,303, Nov. 20, 1984, Programmable controller; Salvatore R. Provanzano, et al., 364/900, 147, 926.9, 927.2, 927.83, 928, 929.2, 933, 933.4, 933.7, 940, 940.1, 940.2, 940.4, 940.61, 940.64, 940.71, 942.3, 942.5, 946.2, 948.3, 948.34, 949, 949.3, 953, 953.4, 962, 964, 964.2, 964.29, 965, 965.4, 965.5, 965.78, 970, 970.5 [IMAGE AVAILABLE]

US PAT NO: 4,484,303 [IMAGE AVAILABLE] L2: 28 of 30
DATE FILED: Jul. 20, 1981

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d 11 1-10 cit,fd,ab

1. 5,043,886, Aug. 27, 1991, Load/store with write-intent for write-back caches; Richard T. Witek, et al., 364/200, 228.1, 228.3, 243.4, 243.41, 243.44 [IMAGE AVAILABLE]

US PAT NO: 5,043,886 [IMAGE AVAILABLE] L1: 1 of 10
DATE FILED: Sep. 16, 1988

ABSTRACT:
A method for reading data blocks from main memory by central processing units in a multiprocessor system containing write-back caches. Load or gather instructions contain a write-intent flag. The status of the write-intent flag is determined. It is also determined whether a data block requested in the instruction by one of the processors is located in a corresponding cache, and if so, the requested data block is returned to the processor. If the data block is not in the cache and the write-intent flag indicates that the block will not be modified, the data block is read from main memory without obtaining a write privilege. The requested data block is subsequently returned from the cache to the processor. If the data block is not in the cache and the write-intent flag indicates the data block will be modified by the processor, then the data block is read from main memory while obtaining the write privilege. Subsequently, the requested data block is returned from the cache to the processor.

2. 5,038,277, Aug. 6, 1991, Adjustable buffer for data communications in a data processing system; Barbara H. Altman, et al., 364/200, 238.4, 238.6, 239, 239.7 [IMAGE AVAILABLE]

US PAT NO: 5,038,277 [IMAGE AVAILABLE] L1: 2 of 10
DATE FILED: Jan. 12, 1990

ABSTRACT:
A data handling system for transferring data between two units, the data being transferred in blocks of a selected number of data words, up to predetermined maximum number. A buffer stores the data being transferred. The buffer includes a plurality of stages arranged serially from an input end to an output end, the number of stages being equal in number to the predetermined maximum number of data words that may be transferred in a block. If the number of data words being transferred is less than the predetermined maximum number, as indicated by a control signal from the unit transmitting the data, the buffer either receives the data in the stage a number of stages from the output end, or transmits the data from the stage a number of stages from the input end, equal to the number of words being transferred in the block.

3. 5,003,463, Mar. 26, 1991, Interface controller with first and second buffer storage area for receiving and transmitting data between I/O bus and high speed system bus; Richard W. Coyle, et al., 364/200, 228.5, 238, 238.3, 239, 239.4, 239.6, 239.7, 240, 240.3, 251.3, 270.2 [IMAGE AVAILABLE]

US PAT NO: 5,003,463 [IMAGE AVAILABLE] L1: 3 of 10

ABSTRACT:
An information processing system comprises a high speed noninterlocked system bus 12 which couples together a plurality of system units including a main memory and a system bus interface (SBI) unit 34. The system bus interface unit is further coupled to an I/O bus 42 having a plurallity of I/O Processors 44, 46 coupled thereto. The system bus interface includes read and write buffer storage for buffering information units being transferred between the system bus and the I/O bus. The I/O bus includes two signal lines which differentiate the condition of an I/O bus SBI BUSY signal line. One of these two signal lines indicates when the SBI read buffer is full while the other signal line indicates when the SBI write buffer is full. The SBI Busy signal line indicates when either of these conditions exist. I/O processors are enabled to differentiate between read and write buffer full conditions, thereby effectively increasing the bandwidth of the I/O bus.

4. 4,977,498, Dec. 11, 1990, Data processing system having a data memory interlock coherency scheme; Joseph Rastegar, et al., 364/200, 238.4, 243.4, 243.41, 246.8, 900, 964.2, 968, 969.2 [IMAGE AVAILABLE]

US PAT NO: 4,977,498 [IMAGE AVAILABLE] L1: 4 of 10
DATE FILED: Apr. 1, 1988

ABSTRACT:
This invention is directed to a memory system that determines which blocks of a set of associative blocks in cache memory are unavailable for replacement. This is accomplished by operating the memory system to maintain a duplicate set of tags which track block ownership for this cache pursuant to a "snoopy" protocol. In addition, the cache system maintains a bit associated with each memory address to indicate whether any data blocks resident in it have been locked. The interlock status of the data blocks in the cache is not communicated to the memory system. Once a block is locked, it cannot be allocated for replacement until it is unlocked. When the cache system encounters a locked block, it skips over that block and allocates the next block of the associative blocks. From this, the memory system infers, by means of a replacement algorithm, that block is being locked and, therefore, cannot be replaced. This enables the memory system to implement an irregular replacement policy for this cache when the block to be replaced is owned and locked.

5. 4,939,641, Jul. 3, 1990, Multi-processor system with cache memories; Martin J. Schwartz, et al., 364/200, 243.4, 243.41, 259.2 [IMAGE AVAILABLE]

US PAT NO: 4,939,641 [IMAGE AVAILABLE] L1: 5 of 10
DATE FILED: Jun. 30, 1988

ABSTRACT:
A system is described wherein a CPU, a main memory means and a bus means are provided. Cache memory means is employed to couple the CPU to the bus means and is further provided with means to indicate the status of a data unit stored within the cache memory means. One status indication tells whether the contents of a storage position have been modified since those contents were received from main memory and another indicates whether the contents of the storage position may be present elsewhere memory means. Control means are provided to assure that when a data unit from a CPU is received and stored in the CPU's associated cache memory means, which data unit is indicated as being also stored in a cache memory means associated with another CPU, such CPU data unit is also written into main memory means. During that process, other cache memory means monitor the bus means and update its corresponding data unit. Bus monitor means are provided and monitor all writes to main [redacted]ory and reads from main memory to aid in the assurance of system-wide [redacted] integrity.

transfer of data from the array to the controller.

=> d l3 1-7 cit,fd,ab

1. 4,965,717, Oct. 23, 1990, Multiple processor system having shared memory with private-write capability; Richard W. Cutts, Jr., et al., 364/200. 228.1, 228.3 [IMAGE AVAILABLE]

US PAT NO: 4,965,717 [IMAGE AVAILABLE] L3: 1 of 7
DATE FILED: Dec. 13, 1988

ABSTRACT:
A computer system in a fault - tolerant configuration employs multiple identical CPUs executing the same instruction stream, with multiple, identical memory modules in the address space of the CPUs storing duplicates of the same data. Memory references. The multiple CPUs are loosely synchronized, as by detecting events such as memory references and stalling any CPU ahead of others until all execute the function simultaneously; interrupts can be synchronized by ensuring that all CPUs implement the interrupt at the same point in their instruction stream. Memory references by the multiple CPUs are voted by each of the memory modules. A private-write area is included in the shared memory space in the memory modules to allow functions such as software voting of state information unique to CPUs. All CPUs write state information to their private-write area, then all CPUs read all the private-write areas for functions such as detecting differences in interrupt cause or the like.

2. 4,942,579, Jul. 17, 1990, High-speed, high-capacity, fault - tolerant error-correcting storage system; Theodore J. Goodlander, et al., 371/51.1; 364/246.4, 266.3, 268.5; 371/10.1 [IMAGE AVAILABLE]

US PAT NO: 4,942,579 [IMAGE AVAILABLE] L3: 2 of 7
DATE FILED: Feb. 27, 1989

ABSTRACT:
A storage system for dynamic and trasparent error correction has a number of first individual storage devices for information and a second individual storage device for error code bits that are used to correct the information when one of the storage devices detects an error. Each error code bit is generated from the information at respective bit positions across the first storage devices. Storage device controllers are connected between a user CPU interface and respective storage devices for operating them concurrently. The interface includes an interface CPU for controlling the storage device controllers and translating the interface convention of user CPU requests into the interface convention of the storage devices. A buffer memory is connected to data surface associated with the respective storage devices. The interface CPU includes logic for immediately acknowledging a write to the associated storage device upon the data being placed in the buffer memory. The interface CPU also includes logic for checking data in the buffer memory and indicating it as having been read from an associated storage device without an actual read, whereby the buffer memory acts as a cache .

3. 4,905,141, Feb. 27, 1990, Partitioned cache memory with partition look-aside table (PLAT) for early partition assignment identification; James G. Brenza, 364/200, 243.41, 243.42, 243.43, 243.44, 243.45 [IMAGE AVAILABLE]

US PAT NO: 4,905,141 [IMAGE AVAILABLE] L3: 3 of 7
DATE FILED: Oct. 25, 1988

ABSTRACT:
A CPU has N-1 ports for concurrently making memory requests and

includes a cache directory partition and a corresponding cache data store partition. Each port has a Partition Look-Aside Table (PLAT). Each PLAT has multiple entries that store the most-recent valid memory requests made by its CPU port. A PLAT entry includes a cache partition identifier, a control field, and a congruence-class address for locating associated data in the identified partition. Simultaneous cache accessing in up to N-1 different partitions may be made by N-1 CPU requests have PLAT local hits. The Nth port services global cache misses. An address switch simultaneously connects the CPU requests to up to N different partitions. A PLAT "local hit" occurs when a CPU request equals PLAT valid entry, enabling immediate accessing of the requested data in the identified partition. A PLAT "miss" generates a "global" request sent to all partitions. If the global request is found in any partition, a global "hit" occurs, and the data is transferred to the requesting CPU port through a data bus switch, and the port's PLAT is validated. If the global request is not found in any partition, a global "miss" occurs, which is sent to the system memory hierarchy for a data fetch; LRU circuits select a partition for receiving the data fetch, and a new PLAT entry is generated for the requesting port.

4. 4,837,739, Jun. 6, 1989, Telemetry data processor; David C. McGill, et al., 364/900; 340/825.05; 364/925, 925.1, 925.6, 927.2, 927.92, 927.93, 929.2, 930, 931, 931.4, 931.44, 932.8, 935, 935.2, 935.4, 935.45, 935.46, 937.01, 940, 940.61, 940.62, 942, 942.04, 943.9, 945, 948.1, 948.3, 948.4, 948.5, 952, 952.1, 959.1, 964, 964.2, 964.34, 965, 965.4, 965.5, 965.76, 965.77, 966.1, 966.3, 968, 972, 976; 370/85.1, 94.1; 371/8.2 [IMAGE AVAILABLE]

US PAT NO: 4,837,739 [IMAGE AVAILABLE] L3: 4 of 7
DATE FILED: Jul. 25, 1986

ABSTRACT:
A telemetry data processor for processing extremely high bandwidth data such as that associated with telemetry from spacecraft. A demultiplexer (1) distributes the data onto several channels (CH1 through CHn), each comprising a (preferably split-cycle synchronous) processing bus (BUS1 through BUSn). Processing can occur on each of the n buses simultaneously. Several processor modules (P boards) are directly coupled to each processing bus, with each P board directly coupled to two buses. Several memory modules (M boards) are directly coupled to each processing bus, with each M board directly coupled to two buses. The functions and architectures of the P boards and M boards are described, along with those of D boards (disk controller modules) and I boards (modules for interfacing the telemetry data processor with its outside environment, which may comprise local area networks, peripherals, gateways, etc.).

5. 4,819,159, Apr. 4, 1989, Distributed multiprocess transaction processing system and method; Dale L. Shipley, et al., 364/200, 230.6, 236.3, 238.4, 238.5, 239, 239.7, 242.4, 242.6, 242.92, 242.94, 242.95, 244, 244.8, 248.1, 265, 266.3, 267, 267.2, 267.4, 268, 268.3, 268.4, 268.5, 268.7, 268.9, 269.2, 269.3, 280, 281.3, 281.8, 282.1, 282.4; 371/9.1 [IMAGE AVAILABLE]

US PAT NO: 4,819,159 [IMAGE AVAILABLE] L3: 5 of 7
DATE FILED: Aug. 29, 1986

ABSTRACT:
The method and means of fault - tolerant processing includes a plurality of system building blocks, each including a real-time processor and specialized processors and local non-volatile memory that are coupled to communicate internally within each of the system building blocks, which, in turn, communicate with one another over local-area network links, and communicate with the remainder of the system over an I/O bus controlled by an I/O processor. Transaction-based processing is under control of a transaction coordinator which permits all of the transaction

US PAT NO: 4,794,521 [IMAGE AVAILABLE] L1: 8 of 10
DATE FILED: Jul. 22, 1985

ABSTRACT:
A cache memory capable of concurrently accepting and working on completion of more than one cache access from a plurality of processors connected in parallel. Current accesses to the cache are handled by current-access-completion circuitry which determines whether the current access is capable of immediate completion and either completes the access immediately if so capable or transfers the access to pending-access-completion circuitry if not so capable. The latter circuitry works on completion of pending accesses; it determines and stores for each pending access status information prescribing the steps required to complete the access and redetermines that status information as conditions change. In working on completion of current and pending accesses, the addresses of the accesses are compared to those of memory accesses in progress on the system.

9. 4,783,736, Nov. 8, 1988, Digital computer with multisection cache; Michael L. Ziegler, et al., 364/200, 228.3, 229, 229.2, 230, 230.1, 231.9, 234, 243, 243.4, 246, 246.4, 263 [IMAGE AVAILABLE]

US PAT NO: 4,783,736 [IMAGE AVAILABLE] L1: 9 of 10
DATE FILED: Jul. 22, 1985

ABSTRACT:
A digital computer including a plurality of memory elements, the memory elements being interleaved (i.e., each is assigned memory addresses on the basis of a low order portion of the memory address), a plurality of processors connected in parallel, the processors each having means for initiating an access of data from any of the memory elements simultaneously with accesses of other processors, the memory elements each being capable of accepting an access from just one of the processors during a given cycle, and the memory elements being interleaved so that the memory access patterns generated at a stride of one and a stride of two each meet the conditions that (1) the pattern will tolerate being offset with respect to an identical pattern by a desired offset and any multiple of the offset (wherein tolerating means that no memory access conflicts arise, i.e., more than one processor simultaneously attempting to access the same memory element) and (2) the pattern includes sufficient conflicts at offsets other than the desired offset to force the processors to assume a relationship wherein the desired offset is achieved, so that the processor is able to access a different memory element simultaneously without creating access conflicts.

10. 4,700,330, Oct. 13, 1987, Memory for a digital data processing system including circuit for controlling refresh operations during power-up and power-down conditions; Barbara H. Altman, et al., 365/222; 364/900, 926.92, 948.5, 964.9 [IMAGE AVAILABLE].

US PAT NO: 4,700,330 [IMAGE AVAILABLE] L1: 10 of 10
DATE FILED: Oct. 30, 1985

ABSTRACT:
A memory for use in a digital data processing system, the memory including a memory controller and one or more memory arrays. A memory array performs refresh operations transparently to the memory controller, but in synchronization with a system timing signal while it is receiving normal system power. A memory array also includes asynchronous refresh circuitry for controlling refresh while the system power is interrupted and the array receives no system timing signal. When each refresh operation occurs during power interruption, the asynchronous refresh circuitry tests the condition of the sys[illegible] power supply. Since refresh operations are transparent to the memory [illegible]ntroller, the memory array indicates when the memory operations are completed. If the memory

al., 364/200, 221, 221.1, 228.1, 229, 229.2, 230, 230.2, 238.3, 238.4, 239, 239.7, 241.2, 242.3, 242.31, 242.6[redacted]2.91, 243, 243.4, 243.41, 247, 247.4, 254, 254.3, 260, 260.3, 265, 265.[redacted]265.3 [IMAGE AVAILABLE]

US PAT NO: 4,912,632 [IMAGE AVAILABLE] L1: 6 of 10
DATE FILED: Mar. 31, 1988

ABSTRACT:
The memory control subsystem controls and arbitrates access to a memory shared by a plurality of users. A processor with its cache and input/output devices has direct access to the memory through a direct memory access bus.
The controls subsystem comprises a processor controller, a DMA controller and a memory controller.
A processor request is buffered into the processor controller and is serviced immediately if the memory controller is available. A simultaneous transfer between the devices and buffers in the DMA controller is possible. If the memory controller is busy, the DMA controller causes the DMA transfer to be interrupted, the processor request to be serviced and the DMA transfer to be resumed afterwards. Write requests made by the processor are buffered into processor controller and an acknowledgement signal is sent to the processor which can resume execution without waiting the memory update completion. A read request which does not hit the cache is sent to the processor controller which causes the cache to be updated.
In case of multiple processor requests contending with a long DMA transfer, the latter is sliced into several parts, each part mapping one cache line. In case of a DMA write, the cache lines which correspond to memory positions whose content is modified by the write operation are invalidated in such a way that the processor cannot read a partially written line into the cache.

7. 4,858,111, Aug. 15, 1989, Write - back cache system using concurrent address transfers to setup requested address in main memory before dirty miss signal from cache; Steven C. Steps, 364/200, 238.3, 238.6, 239.5, 243, 243.4, 243.41, 247, 247.4, 259.2, 263 [IMAGE AVAILABLE]

US PAT NO: 4,858,111 [IMAGE AVAILABLE] L1: 7 of 10
DATE FILED: Oct. 20, 1986

ABSTRACT:
A computer system in which only the cache memory is permitted to communicate with main memory and the same address being used in the cache is also sent at the same time to the main memory. Thus, as soon as it is discovered that the desired main memory address is not presently in the cache, the main memory RAMs can be read to the cache without being delayed by the main memory address set up time. In addition, since the main memory is not accessable other than from the cache memory, there is also no main memory access delay caused by requests from other system modules such as the I/O controller. Likewise, since the contents of the cache memory is written into a temporary register before being sent to the main memory, a main memory read can be performed before doing a writeback of the cache to the main memory, so that data can be back to the cache in approximately the same amount of time required for a normal main memory access. The result is a significant reduction in the overhead time normally associated with cache memories.

8. 4,794,521, Dec. 27, 1988, Digital computer with cache capable of concurrently handling multiple accesses from parallel processors; Michael L. Ziegler, et al., 364/200, 228.1, 228.2, 228.7, 228.9, 232.21, 243, 243.4, 243.41, 243.44, 243.6, 246, 246.3, 246.4, 247, 247.2, 247.3, 254, 254.3, 254.4, 256.3, 256.4, 258, 258.1, 258.2, 258.3, 258.4, 261.3, 261.6, 262, 262.1, 262.4, 262.8, 264, 264.1, 271.5, 280, 280.2, 281.3, 281.4, 281.7 [IMAGE AVAILABLE]

completed transaction, or not to alter any stored data if a transaction is not completed. The transaction coordinator maintains a record of the distributed file accesses required during processing of a transaction, and prevents other transactions from altering stored data during processing of a transaction.

6. 4,625,081, Nov. 25, 1986, Automated telephone voice service system; Lawrence A. Lotito, et al., 379/88, 196, 211; 902/2, 39

US PAT NO: 4,625,081 L3: 6 of 7
DATE FILED: Nov. 30, 1982

ABSTRACT:
An automated telephone voice service system includes a data store having a plurality of addressable voice storage message baskets defined therein and a control system coupled between the store and a large plurality of telephone lines of a telephone network. An incoming cable may address a particular message basket by entering a code through the telephone keyboard or by a predetermined association with a particular call in line. Upon identification of the message basket the caller is greeted by a client's own voice and invited to leave a voice message which will be recorded in the message basket or given other client information. Upon entry of a personal identification code a caller is granted access to user account functions which include retrieval of voice messages, forwarding of messages to other message baskets or telephone lines, and administrative functions such as the changing of greetings or account operating criteria. Editing commands may be utilized during the recording of voice messages.

7. 4,608,688, Aug. 26, 1986, Processing system tolerant of loss of access to secondary storage; Robert C. Hansen, et al., 371/11.3; 364/200, 241.9, 242.3, 242.31, 243.4, 243.41, 245, 245.4, 246.6, 246.8, 263.3, 265, 266, 266.6, 267, 267.8, 268, 268.1, 268.3, 268.4, 268.5, 268.6, 268.8, 268.9, 280, 280.2 [IMAGE AVAILABLE]

US PAT NO: 4,608,688 [IMAGE AVAILABLE] L3: 7 of 7
DATE FILED: Dec. 27, 1983

ABSTRACT:
In a processing system (100) that swaps processes between a main memory (114 or 124) and a pair of duplicated disks (132, 142), system processing capability is protected against loss of access to both system-essential duplicated disks. Upon loss of access to one duplicated disk, processes designed as essential to the system's operation and not resident in the main memory are swapped into the main memory from the other duplicated disk. All essential processes are then locked into the main memory to prevent their removal therefrom. Thus the essential processes remain accessible to the processing system even upon loss of access to both of the disks. Upon loss of access to both of the disks, the system may undergo reconfiguration in an attempt to regain access to at least one of the disks. If reconfiguration fails, non-essential processes are killed and the system continues processing using only the essential processes. Upon restoration of access to one of the disks, the restored disk is initialized from tape and the system is then bootstrapped from the restored disk, and normal processing is resumed. Upon restoration of access to the second disk, the second disk is repopulated from the first disk and the essential processes are unlocked from the main memory.

a digital wireless system; David N. Critchlow, et al., 375/97; 328/155; 375/120

14. 4,881,240, Nov. 14, 1989, AM equalizer circuit for digital systems; David N. Critchlow, et al., 375/15; 333/18; 375/13

15. 4,825,448, Apr. 25, 1989, Subscriber unit for wireless digital telephone system; David N. Critchlow, et al., 375/8; 332/103; 375/56, 67

16. 4,819,159, Apr. 4, 1989, Distributed multiprocess transaction processing system and method; Dale L. Shipley, et al., 364/200, 230.6, 236.3, 238.4, 238.5, 239, 239.7, 242.4, 242.6, 242.92, 242.94, 242.95, 244, 244.8, 248.1, 265, 266.3, 267, 267.2, 267.4, 268, 268.3, 268.4, 268.5, 268.7, 268.9, 269.2, 269.3, 280, 281.3, 281.8, 282.1, 282.4; 371/9.1 [IMAGE AVAILABLE]

17. 4,794,521, Dec. 27, 1988, Digital computer with cache capable of concurrently handling multiple accesses from parallel processors; Michael L. Ziegler, et al., 364/200, 228.1, 228.2, 228.7, 228.9, 232.21, 243, 243.4, 243.41, 243.44, 243.6, 246, 246.3, 246.4, 247, 247.2, 247.3, 254, 254.3, 254.4, 256.3, 256.4, 258, 258.1, 258.2, 258.3, 258.4, 261.3, 261.6, 262, 262.1, 262.4, 262.8, 264, 264.1, 271.5, 280, 280.2, 281.3, 281.4, 281.7 [IMAGE AVAILABLE]

18. 4,783,736, Nov. 8, 1988, Digital computer with multisection cache ; Michael L. Ziegler, et al., 364/200, 228.3, 229, 229.2, 230, 230.1, 231.9, 234, 243, 243.4, 246, 246.4, 263 [IMAGE AVAILABLE]

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1. 5,057,886, Oct. 15, 1991, Non-volatile memory with improved coupling between gates; Bert R. Riemenschneider, et al., 357/23.5, 54; 365/185 [IMAGE AVAILABLE]

2. 5,051,793, Sep. 24, 1991, Coplanar flash EPROM cell and method of making same; Samuel T. Wang, 357/23.5, 23.1, 23.14, 54 [IMAGE AVAILABLE]

3. 5,050,125, Sep. 17, 1991, Electrically erasable programmable read-only memory with NAND cellstructure; Masaki Momodomi, et al., 365/185, 189.09, 189.11 [IMAGE AVAILABLE]

4. 5,049,515, Sep. 17, 1991, Method of making a three-dimensional memory cell with integral select transistor; Jyh-Cherng J. Tzeng, 437/43, 38, 51, 52, 191, 193, 228, 233, 235 [IMAGE AVAILABLE]

5. 5,043,940, Aug. 27, 1991, Flash EEPROM memory systems having multistate storage cells; Eliyahou Harari, 365/168, 185, 218 [IMAGE AVAILABLE]

6. 5,041,886, Aug. 20, 1991, Nonvolatile semiconductor memory device and manufacturing method thereof; Soo-Cheol Lee, 357/23.5, 54; 365/185 [IMAGE AVAILABLE]

7. 5,040,134, Aug. 13, 1991, Neural network employing leveled summing scheme with blocked array; Chin S. Park, 364/602; 307/201; 364/513; 365/49, 185; 382/30, 33 [IMAGE AVAILABLE]

8. 5,039,941, Aug. 13, 1991, Voltage threshold measuring circuit; Hernan A. Castro, 324/158T, 158D [IMAGE AVAILABLE]

9. 5,036,378, Jul. 30, 1991, Memory device; Chih-Yuan Lu, et al., 357/23.5, 23.11, 41, 42, 46, 59; 365/185 [IMAGE AVAILABLE]

10. 5,033,023, Jul. 16, 1991, High dens[redacted] EEPROM cell and process for making the cell; Steve K. Hsia, et al., [redacted]/185; 357/23.5; 365/104, 238.5 [IMAGE AVAILABLE]

11. 5,029,139, Jul. 2, 1991, Word erasable buried bit line EEPROM; James L. Paterson, 365/218, 185, 238.5 [IMAGE AVAILABLE]

12. 5,028,553, Jul. 2, 1991, Method of making fast, trench isolated, planar flash EEPROMS with silicided bitlines; Agerico L. Esquivel, et al., 437/43; 148/DIG.147; 437/49, 200 [IMAGE AVAILABLE]

13. 5,019,879, May 28, 1991, Electrically-flash-erasable and electrically-programmable memory storage devices with self aligned tunnel dielectric area; Te-Long Chiu, 357/23.5; 365/185; 437/43, 44 [IMAGE AVAILABLE]

14. 5,017,980, May 21, 1991, Electrically-erasable, electrically-programmable read-only memory cell; Manzur Gill, et al., 357/23.5, 54; 365/185 [IMAGE AVAILABLE]

15. 5,012,307, Apr. 30, 1991, Electrically-erasable, electrically-programmable read-only memory; Manzur Gill, et al., 357/23.5, 54; 365/185 [IMAGE AVAILABLE]

16. 5,010,028, Apr. 23, 1991, Method of making hot electron programmable, tunnel electron erasable contactless EEPROM; Manzur Gill, et al., 437/43, 49, 52, 195 [IMAGE AVAILABLE]

17. 5,008,212, Apr. 16, 1991, Selective asperity definition technique suitable for use in fabricating floating-gate transistor; Teh-yi J. Chen, 437/43, 52, 193, 195, 228, 233 [IMAGE AVAILABLE]

18. 4,998,220, Mar. 5, 1991, EEPROM with improved erase structure; Boaz Eitan, et al., 365/185; 357/23.5; 365/51, 218 [IMAGE AVAILABLE]

19. 4,996,668, Feb. 26, 1991, Erasable programmable memory; James L. Paterson, et al., 365/185; 357/23.5; 365/189.01, 230.01 [IMAGE AVAILABLE]

20. 4,994,403, Feb. 19, 1991, Method of making an electrically programmable, electrically erasable memory array cell; Manzur Gill, 437/43; 357/23.5; 437/48, 49, 50, 52, 61 [IMAGE AVAILABLE]

21. 4,970,692, Nov. 13, 1990, Circuit for controlling a flash EEPROM having three distinct modes of operation by allowing multiple functionality of a single pin; Syed Ali, et al., 365/218, 189.01, 189.03, 189.05, 230.02, 230.06 [IMAGE AVAILABLE]

22. 4,964,080, Oct. 16, 1990, Three-dimensional memory cell with integral select transistor; Jyh-Cherng J. Tzeng, 365/185; 357/23.4, 23.5, 55 [IMAGE AVAILABLE]

23. 4,958,317, Sep. 18, 1990, Nonvolatile semiconductor memory device and a writing method using electron tunneling; Yasushi Terada, et al., 365/104, 185, 189.04, 189.05 [IMAGE AVAILABLE]

24. 4,951,103, Aug. 21, 1990, Fast, trench isolated, planar flash EEPROMS with silicided bitlines; Agerico L. Esquivel, et al., 357/23.5, 23.14, 45, 59, 67 [IMAGE AVAILABLE]

25. 4,949,309, Aug. 14, 1990, EEPROM utilizing single transistor per cell capable of both byte erase and flash erase; Kamesawara K. Rao, 365/218; 307/465; 357/23.5; 365/104, 185 [IMAGE AVAILABLE]

26. 4,933,906, Jun. 12, 1990, Non-volatile semiconductor memory device; Yasushi Terada, et al., 365/208, 204, 230.03 [IMAGE AVAILABLE]

27. 4,924,437, May 8, 1990, Erasable programmable memory including buried diffusion source/drain lines and erase lines; James L. Paterson, et al., 365/185; 357/23.5; 365/218; 437/43 [IMAGE AVAILABLE]

28. 4,912,676, Mar. 27, 1990, Erasable programmable memory; James L. Paterson, et al., 365/185; 357/23.5; 365/184, 189.01, 230.01

29. 4,894,802, Jan. 16, 1990, Nonvolatile memory cell for eeprom including a floating gate to drain tunnel area positioned away from the channel region to prevent trapping of electrons in the gate oxide during cell erase; Steve K. Hsia, et al., 365/185; 357/23.5; 365/182

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34. 4,839,705, Jun. 13, 1989, X-cell EEPROM array; Howard L. Tigelaar, et al., 357/23.5, 41, 45; 365/185

35. 4,780,750, Oct. 25, 1988, Electrically alterable non-volatile memory device; Joseph G. Nolan, et al., 357/23.5, 12, 23.6, 41, 54; 365/185

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3. 5,014,235, May 7, 1991, Convolution memory; Steven G. Morton, 364/900, 754, 923.5, 927.8, 939.3 [IMAGE AVAILABLE]

4. 5,005,174, Apr. 2, 1991, Dual zone, fault tolerant computer system with error checking in I/O writes; William F. Bruckert, et al., 371/68.3; 364/200, 268.3 [IMAGE AVAILABLE]

5. 4,996,697, Feb. 26, 1991, Deglitching means for digital communication systems; David N. Critchlow, et al., 375/104; 455/223 [IMAGE AVAILABLE]

6. 4,994,802, Feb. 19, 1991, Subscriber unit for wireless digital telephone system; David N. Critchlow, et al., 341/122, 155 [IMAGE AVAILABLE]

7. 4,953,930, Sep. 4, 1990, CPU socket supporting socket-to-socket optical communications; Bernard Ramsey, et al., 359/118; 357/40; 359/154; 385/147 [IMAGE AVAILABLE]

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9. 4,933,846, Jun. 12, 1990, Network communications adapter with dual interleaved memory banks servicing multiple processors; Donald J. Humphrey, et al., 364/200, 231.4, 238.5, 240, 240.1, 242.94, 242.95, 243, 243.6, 246.4, 270, 271.4; 370/85.1 [IMAGE AVAILABLE]

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15. 4,825,448, Apr. 25, 1989, Subscriber unit for wireless digital telephone system; David N. Critchlow, et al., 375/8; 332/103; 375/56, 67

16. 4,819,159, Apr. 4, 1989, Distributed multiprocess transaction processing system and method; Dale L. Shipley, et al., 364/200, 230.6, 236.3, 238.4, 238.5, 239, 239.7, 242.4, 242.6, 242.92, 242.94, 242.95, 244, 244.8, 248.1, 265, 266.3, 267, 267.2, 267.4, 268, 268.3, 268.4, 268.5, 268.7, 268.9, 269.2, 269.3, 280, 281.3, 281.8, 282.1, 282.4; 371/9.1 [IMAGE AVAILABLE]

17. 4,794,521, Dec. 27, 1988, Digital computer with cache capable of concurrently handling multiple accesses from parallel processors; Michael L. Ziegler, et al., 364/200, 228.1, 228.2, 228.7, 228.9, 232.21, 243, 243.4, 243.41, 243.44, 243.6, 246, 246.3, 246.4, 247, 247.2, 247.3, 254, 254.3, 254.4, 256.3, 256.4, 258, 258.1, 258.2, 258.3, 258.4, 261.3, 261.6, 262, 262.1, 262.4, 262.8, 264, 264.1, 271.5, 280, 280.2, 281.3, 281.4, 281.7 [IMAGE AVAILABLE]

18. 4,783,736, Nov. 8, 1988, Digital computer with multisection cache ; Michael L. Ziegler, et al., 364/200, 228.3, 229, 229.2, 230, 230.1, 231.9, 234, 243, 243.4, 246, 246.4, 263 [IMAGE AVAILABLE]